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Design Of Error Hardened Flip-Flop Withmultiplexer Using Transmission Gates And N-Type Pass Transistors

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Abstract: *AConventional edge triggeredmaster-slave flip-flopis very sensitive to particle that causes anerror. Master latch upsets the logic state with an error, when the clock signal is high whereas the slave latch upsets the logic state when the clock signal is low,resulting in an erroneous output of the flip-flop. Here in this paper a new flip flop is presented which can overcome orcontrol any type of error. Here the terms error,single event upset(SEU) and soft errors represent the same meaning. We use an error detection circuit which is used to detect errors and a multiplexer for generating fault indication signal.An error in the master latch or slave latch can be detected when the clock signal is high or low using error detection circuit. The correct output is being generated by the multiplexer using error indication signal, for more efficient results an n-type pass transistor followed by an inverter was introduced instead of transmission gates.The proposed flip-flop with multiplexer and transmission gate and flip flop with multiplexer and n-type pass transistors have small area, less power dissipation and delay overheads.*

Key words: *Flip-flop, hardened techniques, Soft errors, Multiplexer, N-type pass transistors.*

I. Introduction

As VLSI circuits goes on with the evolution and technologies progress, the level of integration is increased and we can achieve high clock speed. Higher clock speeds, increase in levels of integration and scaling of technology are the reasons for the increase in power consumption. As a result, low power consumption has become a serious issue for modern VLSI circuit implementation. Moreover, performance of transistor has limited the power dissipation, static and dynamic for long term device reliability, and increase in integration. Flip-flop is a data storage element. The operation of flip-flops is done by the clock frequency. When multistage flip-flop is operated with respect to the clock frequency, it goes on with high clock switching activity and then increases latency of time. Therefore the speed and energy performance of circuit is affected. To achieve high-speed and low energy operation various flip-flop classes were proposed. To achieve low power dissipation along with area, a new flip-flop with less number of transistors is being proposed and compared with the conventional flip-flop.

II. Power Dissipation

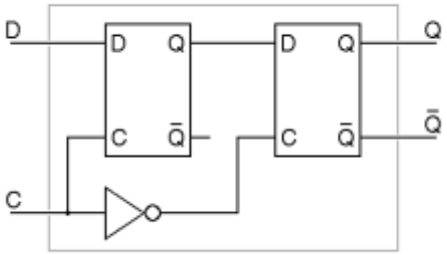
Power dissipation is one of the crucial parameter in the modern VLSI design field. We require consideration for peak power consumption for the design of small devices to ensure performance and proper operation.There are four sources of power dissipations. They are switching power, leakage power, static power and short circuit power.

Feature size scaling and reduction of operating voltages,chips became too sensitive. So,latches and flip flops are susceptible to single event upset(SEU)[1]. These SEU's are also known as soft errorsand these leads to incorrect output. Strike of particlemay affect both flip flops and latches sensitive, which may cause error. Flip flop or latch logic state may be upset during the hold time and these are corrected when a new value is written into it. Single event upset or soft error is nothing but change of state which strikes a particle in electronic devices such as microprocessor,power transistor or semiconductor memory.

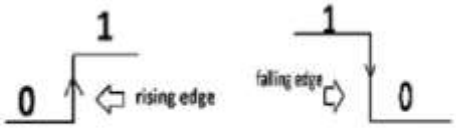
One of the popular techniques Triple Modular Redundancy (TMR) [2]–[5] is used to overcome soft errors, in which three identical modules are used to perform the same function and the results are being compared to generate a single output. If error occurs due to any one of the modules the remaining modules will overcome this error and obtains correct final output. Large area is the main drawback of the TMR, We can say it is upto 200% more area than the actual circuit. Another technique is the error correction code which is widely used against soft errors.A latch can overcome errors to protect the circuit. We can design error hardened latch which can overcome errors by adding additional transistors to its structure, so that its node strength is increased. Hence we can design error hardened flip flops using these latches.

III. Master-Slave Edge-Triggered Flip-Flop

In the master slave edge-triggered flip-flop, master can connect two level sensitive latches to catch the value of the input "D" at Q- when CLK signal is low.Slave latch causes change in clock signal,Q at rising edge.



A rising edge is the low to high transition. It is also known as positive edge. In the rising edge-triggered the circuit becomes active at low to high transitions of clock signals, and avoids the high-to-low transition**.** A falling edge is reverse case where it is the high to low transition. It is called as the negative edge and this avoids low to high transitions.



IV. Conventional rising edge triggered Flip Flop

We know that a conventional master slave flip flop operates when an input given to the master latch, it stores the value and the clock signal transition to the slave latch and generates the output same as the input. In case any error occurs the output may not follow the input. Here in the below circuit there exists fault in the output for which we are going to introduce error detection circuit.

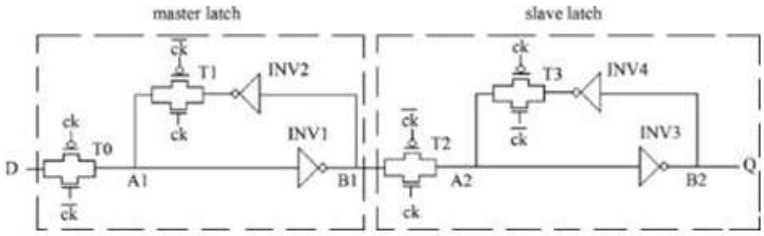


Fig 1: Conventional master slave flip flop

In the below waveforms we can observe the output is faulty as it is exactly the inversion to its input.So modifications must be made for producing error free output.

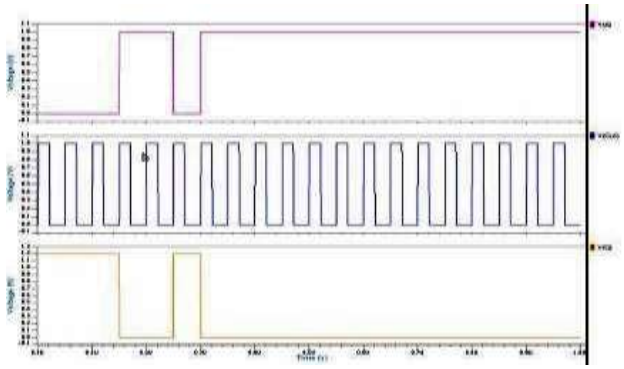


Fig 2: Waveforms of conventional master slave flip flop

The proposed error hardened flip flop uses error detection circuit which consists of two inverters, XNOR gate and a NAND gate with some transistors. This is used to detect errors in the master latch and slave latch. Multiplexer uses fault indication signal,which is indicated by S, to select the correct output. The NAND gate produce logic 1,when the clock signal is low and whereas produces logic 0,when the clock signal changes from low to high during its transition period. When the signal S is pre-charged to logic 1,M1 is turned ON in PMOS,M3 is turned OFF in NMOS.When signal is pre-charged to logic 1,the output values at Q via multiplexer .After rising edge the NAND gate returns to output logic 1 when the clock signal is high .In the reverse case when M1 is OFF in PMOS and M3 is ON in NMOS, the signal selects node Q as final output due to open NMOS M2 at logic 1.

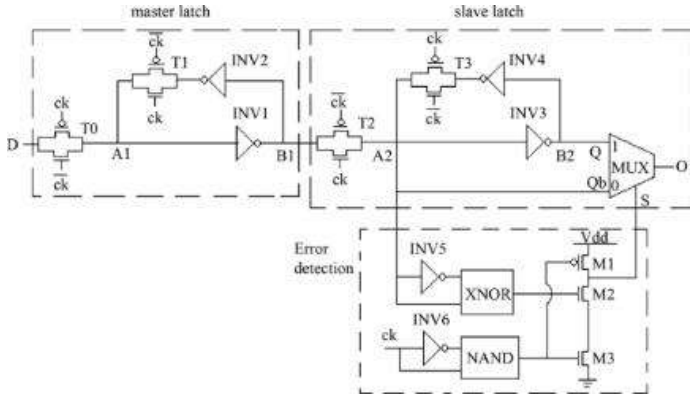


Fig 3: Conventional master slave flip flop with multiplexer

The transmission gate is ON for node A1, 0 TO 1 FOR NODE b1,1 to 0 for node A2.If any difficulty arises it is corrected by the XNOR gate having logic 1 during its invalid transition period. NAND gate produces logic 1,when the clock signal is low .If no error occurs when the clock signal is high,the node Q is selected as final output at logic 1.If any error affects the error detection circuit Qb is selected as final output at logic 0.If the erroneous transition affects the multiplexer 0 is selected as the final outputand it may be erroneous output.

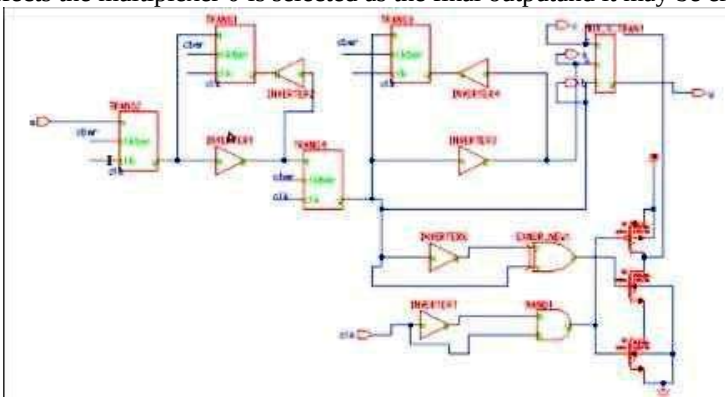


Fig 4: Schematic of conventional master slave flip flop

The waveforms obtained for this conventional master slave flip flop along with the simulation process were as follows

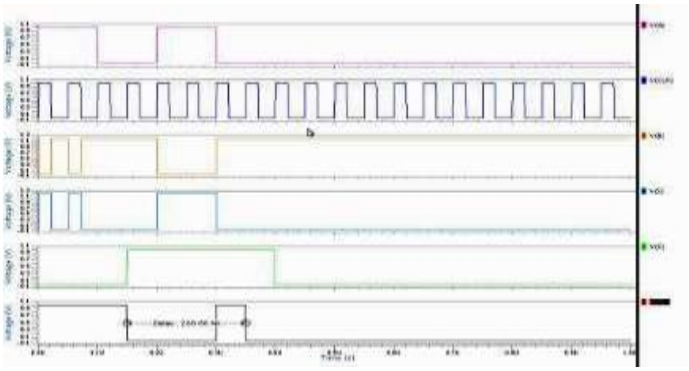


Fig 5: Waveforms of conventional master slave flip flop

Here the delay is 200ns which is high,so we need to concentrate on area and power reduction.Now let us compare our conventional master slave flip flop with a Triple Path Dual Interlocked Storage (TPDICE)[6] flip-flop which uses two TPDICE latches which are used to overcome errors by interlocking internal memory.

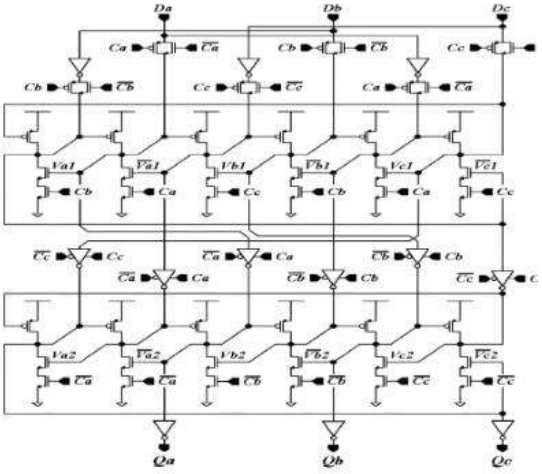


Fig 6 :TPDICE Flipflop

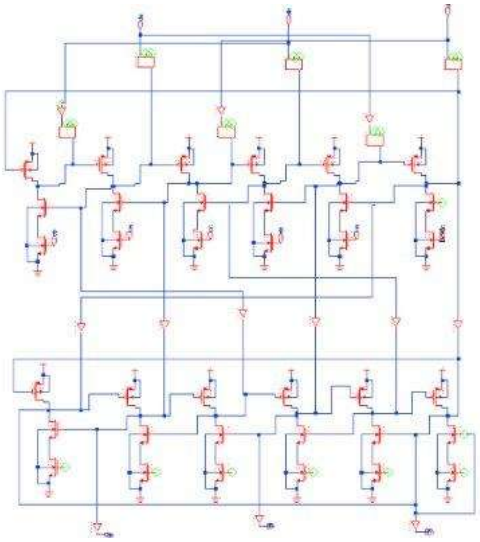


Fig 7: Schematic of TPDICE Flipflop

After the design of TPDICE Flip flop schematic, simulations are being carried out by adding voltages sources to the inputs and as the result, the waveforms obtained are as follows

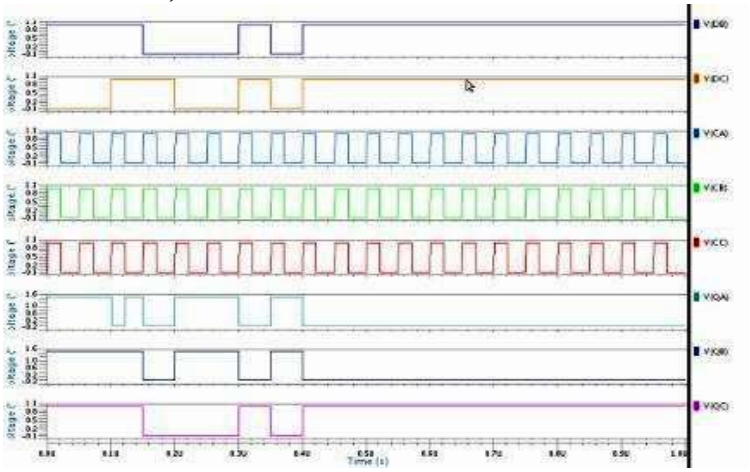
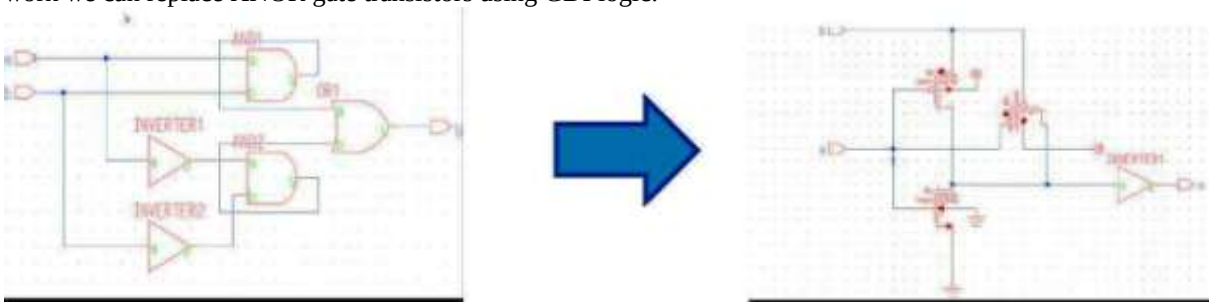


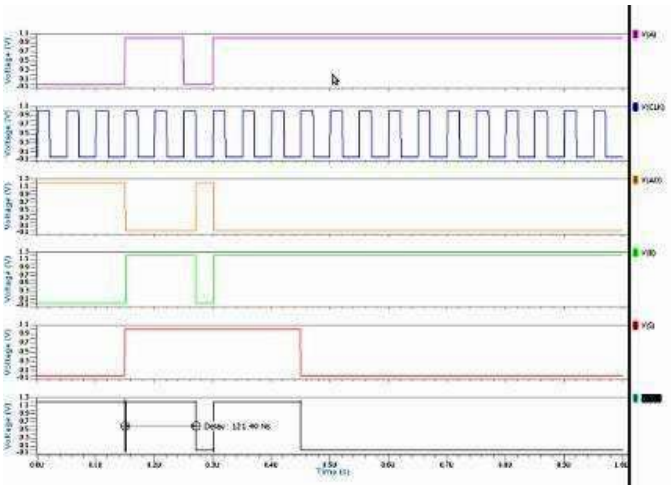
Fig 8: Waveforms of TPDICE Flip flop

So, coming to the conventional master slave flip flop the MUX contains 21 transistors and we are going to replace it with 6 transistors. XNOR is also being replaced with 5 transistors using dynamic logic which is before done with 12 transistors for better area and power performances.

Here we will replace Multiplexer which is having an inverter ,two AND gates and an OR gate with a Multiplexer which is having an inverter and two transmission gates .Here the number of transistors were decreased from 14 to 6.That means less number of transistors and less power consumption.For more effective work we can replace XNOR gate transistors using GDI logic.

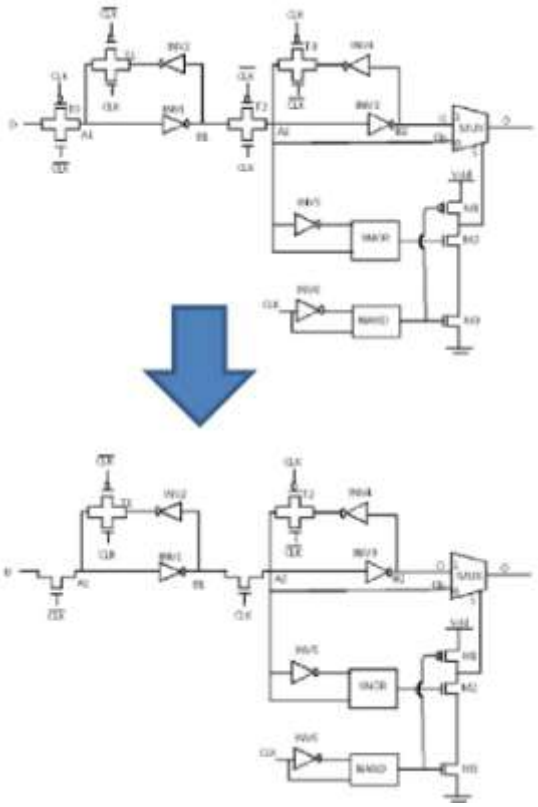


Here there exists great number of decrease in the number of transistors .XNOR is being replaced with another XNOR which is having only 5 transistors as it previously contained two inverters, two AND gates and an OR gate.After replacing the Multiplexer and XNOR with less number of transistors the waveforms obtained are as follows.



Here we can observe that there is tremendous decrease in the delay of the circuit. It came down from 200ns to 121ns.In order to decrease the number of transistors more lesser with less power consumption we had another way to gain it .Two data paths are being used by the low power d flip-flop and the flip-flop .We know that a week high signal is given by the n-type pass transistor, but If this is followed an inverter, it gives strong high. threshold voltage loss of transistors does not exists in the low power d flip-flop .so low power D flip-flop is more efficient in terms of speed, power and area which gives better performance than conventional circuit designs.

The flip flop is as follows



Here we can replace the modified n-type pass transistor flip flop in place of the conventional master slave D flip-flop. The power and area are compared with the existing system.During hold phase, master slave logic state may upset at node A1 or B1 in the faulty output Q. when the clock is low, it locks the erroneous value. Whereas during the hold phase ,the slave latch upsets the results in faulty output Q at node A2 or B2.During the whole clock signal period ,the error hardened flip flop can overcome errors. The error indication signal selects Qb as final output at exact value. Here this flip flop produces small area and less power dissipation.

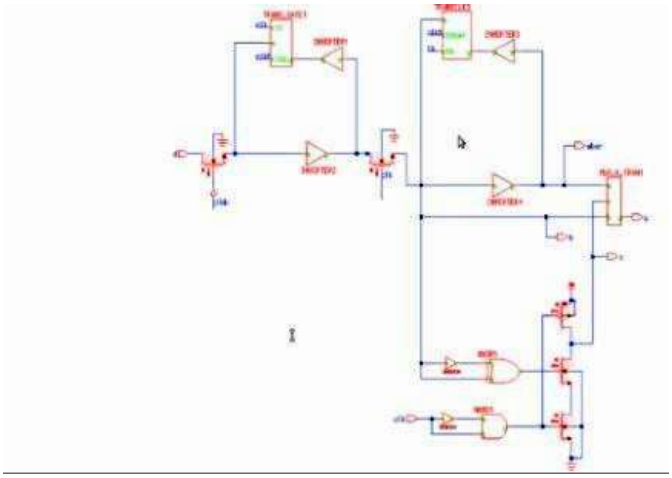
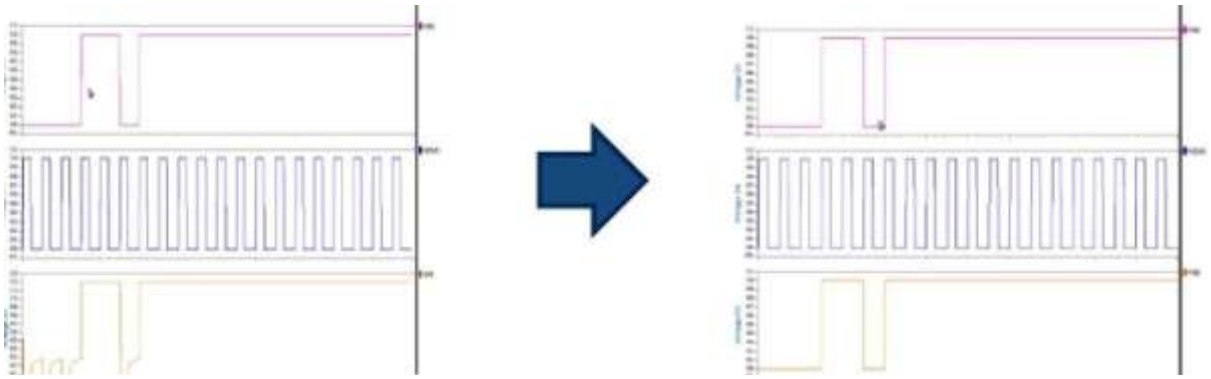


Fig 9: Schematic of flip flop using n-type pass transistor

The waveforms we obtained for the above n-type pass transistor flip flop are as follows



The output comes with delay as we can observe spikes in the above waveforms. We can overcome it by adding a delay element that is, two inverters connected back to back. In the above waveforms we can observe that there are zero spikes which means we got the exact output. But here we introduced delay element which results in the increase of the delay product.

V. Layouts

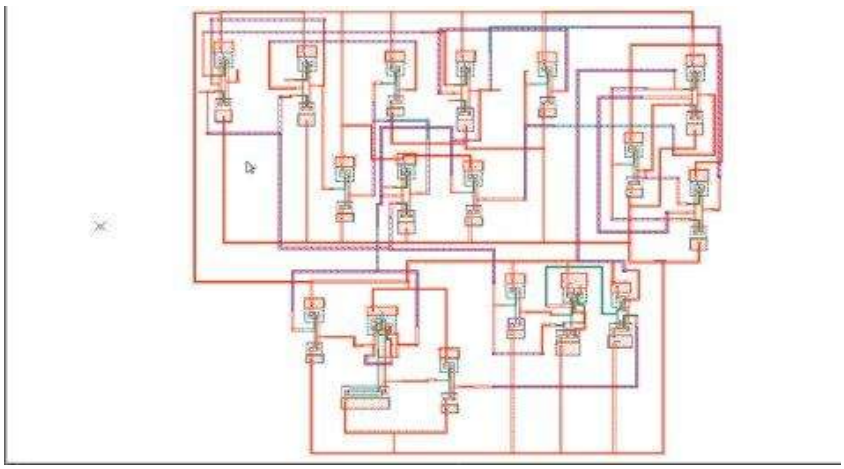


Fig 10: Layout of the conventional master slave flip flopwith multiplexe

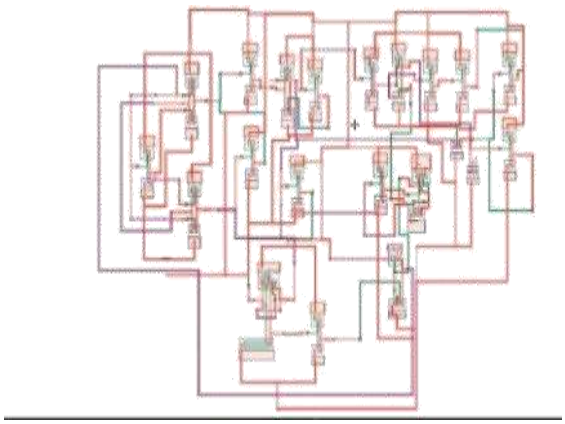


Fig 11: Layout of flip flop with n-type pass transistors

VI. Simulation Results

To compare the performance of proposed flip-flop with existing flip-flop designs, all the circuits are designed using Mentor graphics schematics and layout editor and extracted using 130nm CMOS technology [7]. Simulations were carried using ELDO, with the capacitances and resistances extracted from the layout. These flip-flops are simulated with 2GHz frequency and at 270C and the supply voltage of 1.2V.

Flip-flop	No. Of Transistors	Rise time	Fall time	Power dissipation
TPDICE flip-flop	72	69.541ps	93.865ps	22.654nw
Conventional master slave flip-flop	55	279.86ps	151.91ps	16.781nw
Flip flop with multiplexer and transmission gates	39	121.26ps	96.83ps	13.765nw
Flip flop with multiplexer and n-type pass transistor	37	121.869ps	76.876ps	11.01nw

From the above table, number of transistors and power dissipation of the flip flop using multiplexer and n-type pass transistors is observed to be less when compared with the flip flop using multiplexerandtransmission gate. And number of transistors and power dissipation for the new flip flops proposed is observed to be less in comparison with the conventional master slave flip flop.

VII. Design of Serial In Serial Out (SISO)

One clock per each state will be delayed by the Serial In Serial Out shift registers (SISO).For each register a bit of data will be stored. We have to clear the register first by allowing all the outputs to 0.Then we have to apply each data sequentially. One bit is transmitted from left to right during each clock pulse.

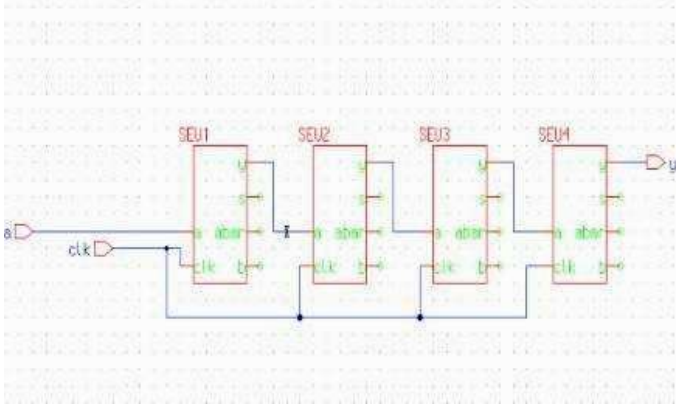


Fig 12: Schematic of SISO design

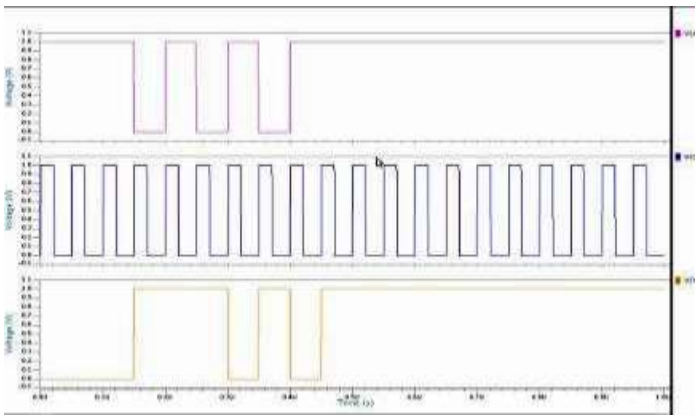


Fig 13: Waveforms of SISO

Here we can observe the data is being shifted after three clock signals and the output is being obtained.

VIII. Conclusion

New less area and low power consumed flip flops are proposed using multiplexerandtransmission gates andflip flop using multiplexer and n-type pass transistors. The proposed flip-flops were compared with the conventional flip-flops and seem to be exhibiting low power dissipation and less area occupation. The proposed flip-flops using multiplexer with transmission gate and flip flop with multiplexer and n-type pass transistors results in reduction in the power dissipation up to 50-60% and area up to 30-50% in comparison with the conventional flip-flops. The SISO shift register designed with proposed flip-flop using multiplexerand transmission gate and flip flop usingmultiplexer andn-type pass transistors exhibits power dissipation reduction. Hence the proposed architectures demonstrates less area and low power dissipation in the circuit where delay overheads.

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